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IASET

DESIGN METHOD AND SIMULATION OF TIQ COMPARATOR BASED ADC

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ABSTRACT

This Paper addresses a Threshold Inverter Quantization (TIQ) based CMOS flash analog-to-digital converter (ADC) for system-on-chip (SoC) applications. However, this TIQ technique must be developed to satisfy recent SoC trends, which force ADCs to be integrated on the chip with other digital circuits and centre on low-power and low-voltage implementations.

Thus, this paper proposes an optimal design method for the TIQ comparator and a new voltage comparator for better implementation in SoC applications. These proposals contributed toward the achievement of high-speed conversion, low-power dissipation, and low-voltage operation in the TIQ flash ADC.

Therefore, we obtained a higher speed and resolution TIQ flash ADC. The results demonstrate that the TIQ flash ADC achieves high-speed conversion, and has a small size, low-power dissipation, and low-voltage operation compared to other flash ADCs.

KEYWORDS: Threshold Inverter, Quantization (TIQ), TIQ Flash ADC

INTRODUCTION

The least amount channel length of the transistor will be scaled down to 0.065 µm in 2007 according to the roadmap of semiconductors In addition to this down- scaling, today's system-on-chip (SoC) trend forces analog and mixed-signal integrated circuits (ICs) to be integrated by means of multifaceted digital processors and memory on a single chip - called complete SoC or digital and mixed-signal SoC.

At present, there are a lot of stress on the entire SoC in wireless and broadband communications - wireless networking, wired com- munication (WAN and LAN), and consumer electronics (DVD, MP3, digital cameras, video games, and so on). Therefore, as one of the mixed-signal ICs, analog-to-digital converters (ADCs) have to follow this whole SoC trend.

ADC PARAMETER

So many parameter for ADC

Static Parameters

The static parameters explain the errors between the actual points and the ideal/theoretical points in the staircase transfer function of an ADC. Figure below shows the staircase transfer function of an ADC. The actual characteristic does not match with the model characteristic in both the reference voltage and the width of horizontal steps, as shown.
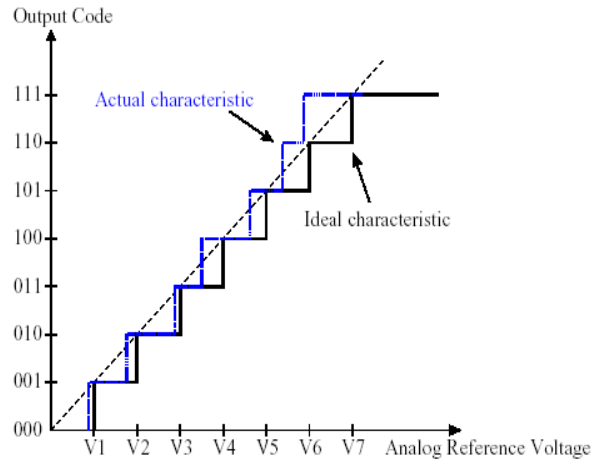
Figure 1

Offset and Gain Error

The offset error, E_{offset}, is defined as the difference between the nominal and actual offset points. This offset error can be mathematically formalized.
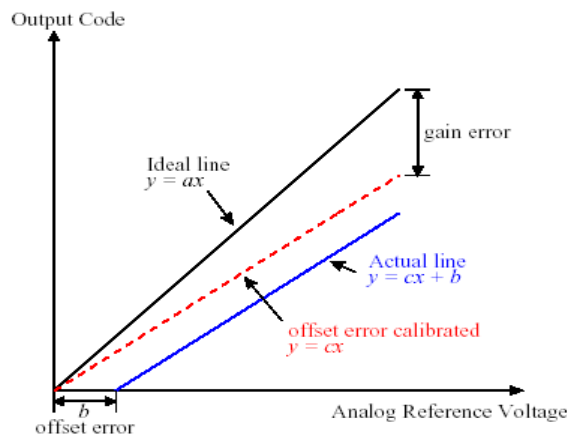

Figure 2

Differential Non-Linearity Error (DNL)

The differential non-linearity error (DNL), sometimes merely called differential Linearity (DLE), describes how far the real step size is from the model step in the least significant bit (LSB) unit, after elimination of the gain error.
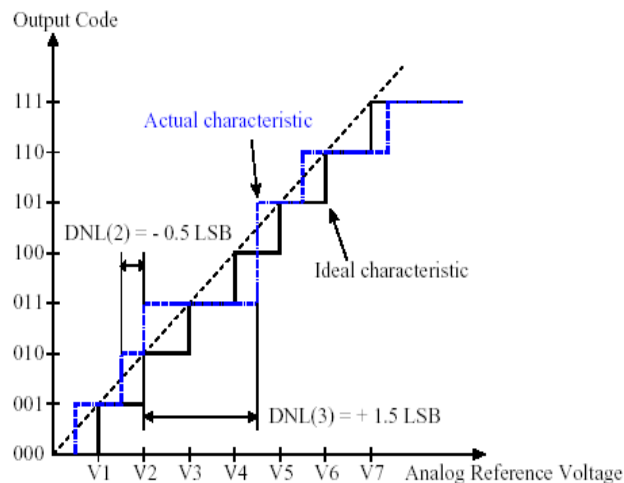

Figure 3

Integral Non-Linearity Error (INL)

The integral non-linearity error (INL), sometimes merely called integral linearity (ILE), checks the dissimilarity between the actual reference voltages and the ideal reference voltages at all transition points.
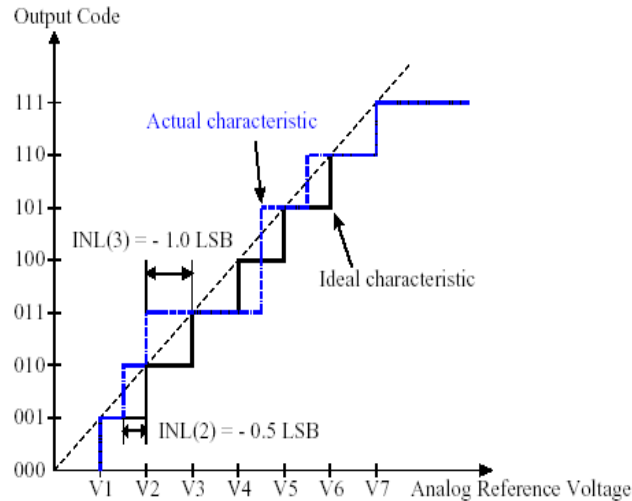

Figure 4

Dynamic Parameters

The static parameters are determined by DC Tests, but the dynamic parameters are concerned with AC specifications such as resolution, sampling frequency, input signal frequency, and so on. The main parameters to review are the signal-to-noise ratio (SNR), the signal-to-noise ratio, the effective number of bits (ENOB).

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio of signal power to noise power. With the SNR, we can easily be familiar with how much noise is added to the signal by an ADC. Generally, the SNR is expressed in decibels (dB).

FLASH ADC

The flash ADC is known for having the fastest speed compared to previous ADC architectures. Therefore, it is used for high-speed and very large bandwidth applications such as radar processing, digital oscilloscopes, high-density disk drives, and so on. The flash ADC is also known as the parallel ADC because of its parallel voltage comparator architecture. This architecture needs $2^n - 1$ comparators for an n-bit ADC. For example, a set of 15 comparators are used for a 4-bit flash ADC. Each comparator has a reference voltage that is provided by an outside reference source.

These reference voltages are equally spaced by VLSB from the major reference voltage (V2n-1) to the smallest number of reference voltage V_1. An analog input is associated to all comparators so that each comparator output is shaped in one cycle. The digital output of the set of comparators – called the thermometer code - is distorted into a binary code through the encoder.

TIQ COMPARATOR

The comparator is the most significant component in the ADC architecture. Its position is to convert an input voltage V_{in} into a logic `1' or `0' by comparing a reference voltage V_{ref} with the V_{in}. If the V_{in} is superior than V_{ref} , the output of the comparator is `1', otherwise `0'. Frequently used comparator structures in CMOS ADC design are the fully differential latch comparator [4] and the dynamic comparator .The former is sometimes called a "clocked comparator," and

the final is called an "auto-zero comparator" or "chopper comparator." To attain high speed, such comparators are typically implemented with bipolar transistor technology. For SoC implementation in this case, BiCMOS technology would be necessary to integrate together a high-speed ADC and a digital signal process on the similar substrate.

The TIQ comparator uses two cascaded CMOS inverters as a comparator for highspeed conversion and low-power dissipation. The proposed TIQ comparator that is described in this report has been developed not only for higher speed but also for higher resolution.

CMOS Inverter as a Comparator

The inverter threshold voltage Vm is defined as the Vin = Vout point in the VTC of an inverter. Mathematically,

$$V_m = \frac{r\left(V_{DD} - |V_{Tp}|\right) + V_{Tn}}{1 + r} \quad \text{with} \quad r = \sqrt{\frac{k_p}{k_n}}$$

where VTp and VTn represent the threshold voltages of the PMOS and NMOS devices, correspondingly. Figure below shows the schematic of the TIQ comparator and its VTC from the simulation. At the first inverter, the analog input signal quantization level is t by
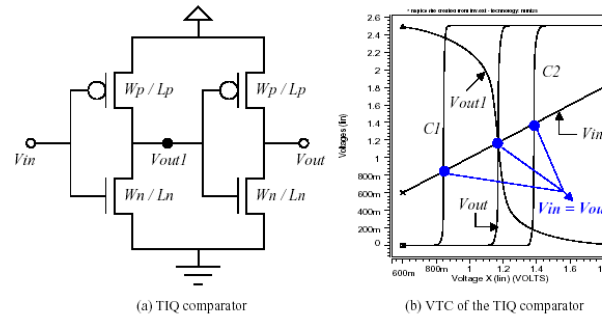

(a) TIQ comparator   (b) VTC of the TIQ comparator

Figure 5

Voltages (l_{in}) V_m, depending on the W/L ratios of PMOS and NMOS. The another inverter is used to increase voltage gain and to prevent an disturbed propagation delay. In Figure 5(b), the slope of V_{out} is shown outsized than that of V_{out1}. The inverter threshold depends on the transistor sizes. The C_1 and C_2 curves show the dissimilarity in the VTC of Vout. With a set length of the PMOS and NMOS devices, we can obtain required values of C1 and C2 by increasing only the width of the PMOS and NMOS transistors, respectively. This result can be confirmed by the following equation of the inverter threshold [2].

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{DD} - |V_{Tp}|\right) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

where μ_p and μ_n are the electron and hole mobility, respectively. To obtain above Equation, we suppose that mutually transistors are in the active region, the gate oxide thickness (C_{ox}) for both transistors is the similar, and the lengths of both transistors (L_p and L_n) are also the similar. From above equation, we know that V_m is shifted, depending on the transistor width ratio (W_p/W_n). That is, growing W_p makes V_m larger, and growing W_n makes V_m lesser on the VTC.

This altering of the widths of the PMOS and NMOS devices with a set transistor length is the thought of the TIQ comparator. We can employ the inverter threshold voltage as an internal reference voltage to evaluate the input voltage.

However, to use the CMOS inverter as a voltage comparator, we have to check the sensitivity of V_m to other parameters, which are ignored in the equation, for right operation of the TIQ flash ADC. In a mixed-signal design, the ignored parameters - threshold voltages of transistors, electron and hole mobility, and power supply voltage - are not permanent at a constant value.

CONVERSION RATE

The time taken for the complete conversion of analog to digital covering all possible combinations i.e. from 0 to 15 is 5 µsec. This show that how we obtain 16 codes in 5 µsec through frequency 0.2MHz (for C_{load} = 1pf). The conversion rate for this Flash ADC is 3.2Msample/sec. This can be seen from the waveform below.

Experimental Evaluations

This is the table for 16:4 encoder. Its output is converted into gray code for simplifying the hardware.

```
 I  I  I  I  I  I I I I I I I I I I                 Y
15 14 13 12 11 1  9 8 7 6 5 4 3 2 1 0  3 Y2 Y1 Y0  G3 G2 G1 G0
 0  0  0  0  0  0 0 0 0 0 0 0 0 0 1 0  0  0  0  0   0  0  0  0
 0  0  0  0  0  0 0 0 0 0 0 0 0 1 X 0  0  0  1      0  0  0  1
 0  0  0  0  0  0 0 0 0 0 0 0 1 X X 0  0  1  0      0  0  1  1
 0  0  0  0  0  0 0 0 0 0 0 1 X X X 0  0  1  1      0  0  1  0
 0  0  0  0  0  0 0 0 0 0 1 X X X X 0  1  0  0      0  1  1  0
 0  0  0  0  0  0 0 0 0 1 X X X X X 0  1  0  1      0  1  1  1
 0  0  0  0  0  0 0 0 1 X X X X X X 0  1  1  0      0  1  0  1
 0  0  0  0  0  0 0 1 X X X X X X X 0  1  1  1      0  1  0  0
 0  0  0  0  0  0 1 X X X X X X X X 1  0  0  0      1  1  0  0
 0  0  0  0  0  1 X X X X X X X X X 1  0  0  1      1  1  0  1
 0  0  0  0  1  X X X X X X X X X X 1  0  1  0      1  1  1  1
 0  0  0  1  X  X X X X X X X X X X 1  0  1  1      1  1  1  0
 0  0  1  X  X  X X X X X X X X X X 1  1  0  0      1  0  1  0
 0  1  X  X  X  X X X X X X X X X X 1  1  0  1      1  0  1  1
 1  X  X  X  X  X X X X X X X X X X 1  1  1  0      1  0  0  1
                                    1  1  1  1      1  0  0  0
```

G3= I8

G2=I4.I'12

G1=I2.I'6 + I10.I'14

G0=I1.I'3 + I5.I'7 + I9.I'11 + I13.I'15

The table below shows the exact W and L for each comparator for different switching point voltage. We have kept W_n= 0.4µ, L_n= 0.18µ, L_p= 0.18µ fixed for theoretical calculations.

Table 1

| V	After Simulation Wp (Microns)	Theoretical Wp (Microns)	After Simulation Lp (Microns)	After Simulation Wn (Microns)	After Simulation Ln (Microns)
V14=1.16	9.95	11.94	0.18	0.400	0.505
V13=1.12	8	7.07	0.18	0.515	0.500
V12=1.08	7	4.44	0.18	0.700	0.450
V11=1.04	5	2.89	0.18	0.400	0.250
V10=1.00	4	1.94	0.18	0.415	0.220
V9=0.96	2.7	1.31	0.18	0.400	0.220
V8=0.92	2	0.904	0.18	0.400	0.215
V7=0.88	1.38	0.629	0.18	0.400	0.220
V6=0.84	1	0.422	0.18	0.400	0.220
V5=0.8	0.87	0.283	0.18	0.400	0.185
V4=0.76	0.63	0.186	0.18	0.400	0.180
V3=0.72	0.44	0.1187	0.18	0.400	0.180
V2=0.68	0.4	0.0714	0.2	0.550	0.180
V1=0.64	0.4	0.03959	0.23	0.920	0.180
V0=0.60	0.4	0.01905	0.2	2.800	0.180
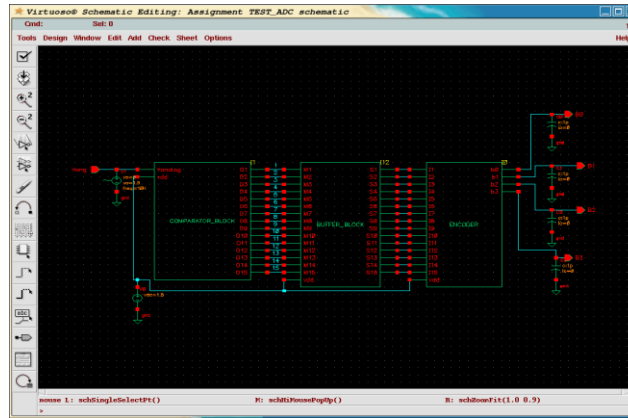
Figure 6: Block Diagram of Flash ADC

This figure shows the block diagram of Flash ADC (4 Bits).It contains the following main blocks: Comparator, buffer & Encoder. The Comparator block contains a total of 15 comparators which compares the input analog signal. The after that block is buffer which makes sure that the voltage swing level is maintained. At last with the help of encoder block the output of comparator is converted to digital equivalent. These blocks are shown below with their detail connections. The figure 7 shows the equivalent digital output for input analog signal.
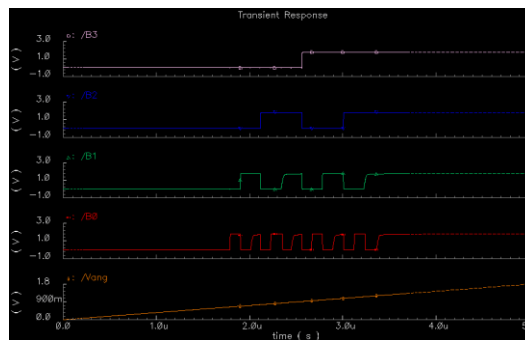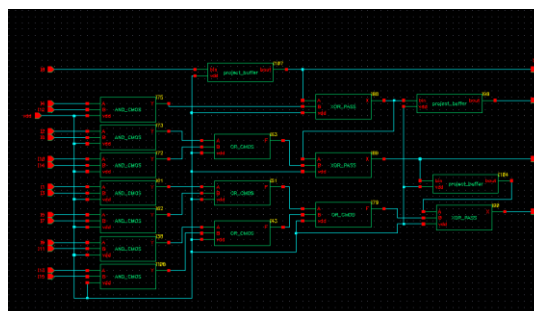

Figure 7

Figure 8: Comparator Schematic Diagram

Figure 9: Encoder Schematic Design
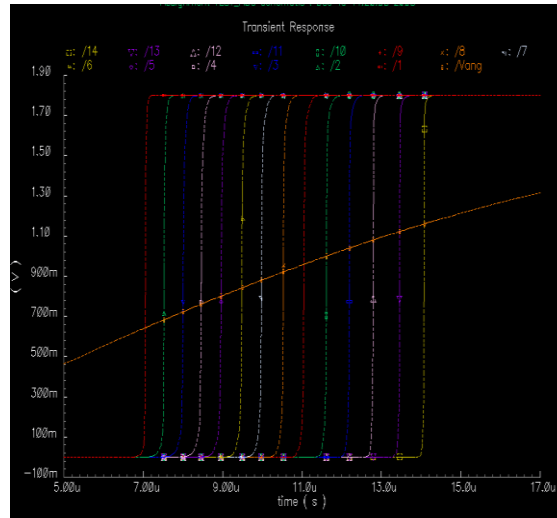
CONCLUSIONS

Figure 10: Transient Response of TIQ Based Comparator
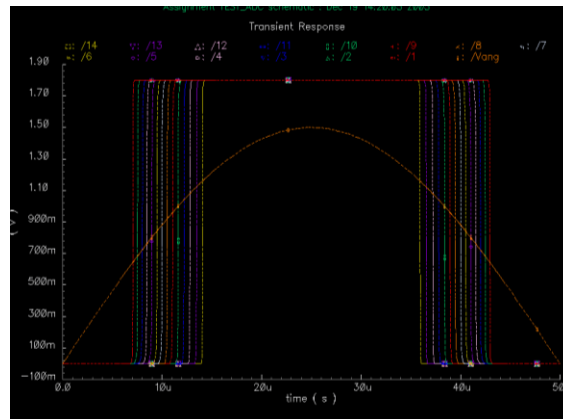

Figure 11: Transient Response of Comparator

A simple and quick flash ADC structural design that uses two cascaded CMOS inverters as a comparator, called Threshold Inverter Quantization (TIQ) technique, has been planned by Ali Tangel. In this paper, a new design method (systematic size variation (SSV) technique) and a novel type of encoder have been developed for advanced TIQ flash ADCs. Their applications can be wideband RF, wireless local loop, radar/communications, universal computer network adaptor, and so on. The TIQ flash ADC offers higher data conversion rates while maintaining a comparable power consumption level so that it is also extremely suitable for the complete SoC integration using the standard digital CMOS process.

In addition to the techniques for improving the performance of the TIQ flash ADCs, two applications of the TIQ technique have been proposed: low power consumption and low voltage operation. Because parallel voltage contrast is used in the flash ADC, the power consumption gets much larger as we augment the resolution of the ADC. With the TIQ comparator feature, we have implemented together the power and resolution adaptive flash ADC and the power management method in the TIQ flash ADC.

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